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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,347	06/20/2005	Jorg Sorg	5367-144PUS	2965
27799 7590 10/09/2007 COHEN, PONTANI, LIEBERMAN & PAVANE 551 FIFTH AVENUE SUITE 1210 NEW YORK, NY 10176			EXAMINER TRAN, THANH Y	
			ART UNIT 2822	PAPER NUMBER
			MAIL DATE 10/09/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/519,347

Applicant(s)

JONG SORG

Examiner

Thanh Y. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, and 3-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5, 9, 12-13, and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hohn et al (U.S. 6,066,861).

As to claim 1, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode comprising: a chip package which has a leadframe (2, 3, 8), and a semiconductor chip ("semiconductor body" 1) which is arranged on, and is in electrical contact with, the leadframe (2, 3, 8) and which contains an active, radiation-emitting and/or radiation-receiving region (see col. 4, lines 42-61), wherein the leadframe (2, 3, 8) is formed by a flexible multi-layered sheet that comprises a metal foil (2/3) and a plastic film (a plastic film can be a plastic layer of 8 underneath layers 2, 3), the plastic film being arranged on, and connected to, the metal foil (2/3).

As to claim 3, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package, wherein the plastic film (8) is adhesively bonded to the metal foil (2, 3).

As to claim 5, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package, wherein the semiconductor chip ("semiconductor body" 1) comprises a first contact area (as indicated at 11 in figures 1-2) on the first chip

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connection region (region of element 2), and a second contact area (as indicated at 12 in figures 1-2) coupled to the second chip connection region (region of element 3).

As to claim 9, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package, wherein the semiconductor chip ("semiconductor body" 1) is embedded in an encapsulating material (5).

As to claim 12, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, comprising: providing a leadframe (2, 3, 8) from a flexible multi-layered sheet (a flexible multi-layered sheet comprising layers 2, 3, and a layer of 8 underneath layers 2, 3) which has a first chip connection region (region of element 2) and a second chip connection region (region of element 3), the flexible multi-layered sheet that comprises a metal foil (2/3) and a plastic film (a plastic film can be a plastic layer of 8 underneath layers 2, 3), the plastic film being arranged on, and connected to, the metal foil (2/3); providing a semiconductor chip ("semiconductor body" 1), which contains an active, radiation-emitting region (see col. 4, lines 42-61) and has a first contact area (as indicated at 11 in figures 1-2) and a second contact area (as indicated at 12 in figures 1-2); mounting the semiconductor chip (1) with the first contact area (11) on the first chip connection region of the leadframe (2, 3, 8); connecting the second contact area (12) to the second chip connection region of the leadframe (2, 3, 8); and encapsulating the semiconductor chip (1) with a transparent or translucent encapsulating material ("casting composition" 5 is based on "a transparent epoxy casting resin", see Abstract in Hohn et al).

As to claim 13, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein the

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step of providing a leadframe (2, 3, 8) comprises providing and punching a thin metal foil (2, 3) in order to define the first and second chip connection regions.

As to claim 15, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein the step of providing a leadframe (2, 3, 8) comprises the adhesive bonding (5) of the foil (2, 3) and the film (8).

As to claim 16, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein in the encapsulating step, the encapsulating material (5) is injection-molded onto the plastic film (8) of the multi-layered sheet.

As to claim 17, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein, in the encapsulating step, a runner is LED through a plurality of chips arranged on the multi-layered sheet (see col. 10, lines 7-12; and col. 8, lines 49-54).

As to claim 18, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein the first and second chip connection regions (regions of elements 2 and 3) of the leadframe are short-circuited and grounded in the steps of mounting the semiconductor chip (1), connecting the second contact area (12) and encapsulating the semiconductor chip (1).

Claim Rejections - 35 USC § 103

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3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohn et al (U.S. 6,066,861) in view of Shirai et al (U.S. 2005/0208789).

As to claims 4 and 14, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package, wherein the metal foil (2, 3) comprises a first chip connection region (region of element 2) and a second chip connection region (region of element 3), and in that the plastic film (8) has an opening in the regions arranged on these chip connection regions (regions of 2 and 3); wherein a leadframe (2, 3, 8) is provided and punched to a thin plastic film (8) for the electrical connection of the semiconductor chip.

Hohn et al does not disclose the plastic film has openings in the regions arranged on these chip connection regions.

Shirai et al discloses in figures 7 and 9 an apparatus comprising: an insulating film (10b) has openings in the regions of the leadframe arranged on these chip connection regions (see chip connection regions in figure 9). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Hohn et al by having an insulating film which has the openings in the regions of the leadframe as taught by Shirai et al for electrically connecting the chips to the leadframe through the openings of the insulating film.

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5. Claims 6-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hohn et al (U.S. 6,066,861).

As to claims 6, 8 and 10-11, As to claim 4, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package, wherein one of the preceding claims, characterized in that the luminescent diode (see col. 10, lines 7-12; and col. 8, lines 49-54).

Hohn et al does not disclose thickness of the metal foil is less than 80 μm ; wherein the thickness of the plastic film is less than 80 μm ; wherein the leadframe has footprint dimensions of approximately 0.5 mm x 1.0 mm or less; the luminescent diode has a total thickness of approximately 400 μm or less. However, *the dimension range for a metal foil or a leadframe; and a desired thickness range for a plastic film or a luminescent diode* would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 7, Hohn et al does not disclose the plastic film comprises an epoxy resin film. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify apparatus of Hohn et al by using epoxy resin film for forming a

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plastic film for providing a good thermally insulating layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hohn et al (U.S. 6,066,861) in view of Fjelstad (U.S. 6,093,584).

As to claim 19, Hohn et al discloses in figure 3 a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein plurality of chips arranged on the multi-layered sheet (comprising layers 2, 3 and a layer of 8 underneath layers 2, 3) is capable of testing for their functional capability after the encapsulating step (5).

Hohn et al does not disclose the apparatus comprising a plurality of chips arranged in the leadframe and wherein the individual chips are electrically isolated when they are mounted.

Fjelstad discloses in figures 1A-1G-1 an apparatus comprising a plurality of chips (121, 120) arranged in the leadframe (102) and wherein the individual chips (121, 120) are electrically isolated when they are mounted (see figure 1G-1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Hohn et al by providing a plurality of individual chips for the purpose of producing/making a plurality of semiconductor devices/packages.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 8, 11, and 12 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that Holn fails to teach that housing 8 is arranged on the metal foil.

In response, the examiner disagrees with applicant's argument because figure 3 of Holn clearly discloses that housing 8 having a layer/portion underneath layers 2 and 3 and it is arranged on the metal foil (2, 3).

Applicant further argued that Holn fails to teach a multilayered sheet that is flexible.

In response, the examiner disagrees with applicant's argument because figure 3 of Holn clearly discloses that a multilayered sheet (comprising layers 2, 3 and a layer of 8 underneath of layers 2 and 3) that has at least a flexible layer (2/3).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT



M. Wilczewski
Primary Examiner
TC 2800